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1	WO 00/51014	31.08.2000	Europe			<input checked="" type="checkbox"/>	
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ATT ↓	2	K. Nakamura et al.; "SP 24.6: A 500 MHz 4Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O" 1997 IEEE International Solid-State Circuits Conference; pages 406, 407, & 495					
	3	M. Fukaiishi et al. "TP 15.7 A 20Gbs CMOS Multi-Channel Transmitter and Receiver Chip Set for Ultra-High Resolution Digital Display;" 2000 IEEE International Solid-State Circuits Conference; pages 260 - 261.					
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4	K. Nakamura et al.; "A 50% Noise Reduction Interface Using Low-Weight Coding;" 1996 Symposium on VLSI Circuits Digest of Technical Papers; pages 144 - 145						
5	K. Nakamura et al. "A 500-MHz 4-Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O;" IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997; pages 1758 - 1765						
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